CLAIMS

1. A nanoscale interconnection interface comprising:

a first number of input address signal lines that carry addresses separated from one another by a first average Hamming distance;

a second number of coded address signal lines; and

a third number of nanowires, each nanowire addressed by one or more coded addresses comprising signals carried by the coded address signal lines and derived from an input address received on the input address signal lines, the internal nanowire addresses separated from one another by a second average Hamming distance greater than the first average Hamming distance.

2. The nanoscale interconnection interface of claim 1 further comprising an encoder that receives an input address through the input address signal lines and outputs a coded address to the coded address signal lines.

3. The nanoscale interconnection interface of claim 2 wherein the coded addresses are derived from codewords corresponding to the input addresses, each input address and corresponding coded address both uniquely identifying one of:

a single nanowire; and

a single subset of the number of nanowires.

4. The nanoscale interconnection interface of claim 2

wherein the first number of input address signal lines is k, the second number of independent, coded address signal lines is n, where $n = k + r$; and

wherein the coded addresses are n-bit codewords derived from a systematic linear block error-control encoding technique, each codeword having k bits equivalent to an input address and r parity check bits and generated by multiplication of the input address by a generator matrix for the linear block code, the coded addresses separated by a minimum Hamming distance greater than 1.

5. The nanoscale interconnection interface of claim 2

wherein the first number of input address signal lines is k, the second number of independent, coded address signal lines is n, where $n > k$; and

wherein the coded addresses are n-bit codewords derived from a combinatoric encoding technique, each codeword representing a selection of a number of bits s having a value "1" within an n-bit codeword, the number of codewords C_s^n greater than or equal to the number of nanowires.

6. The nanoscale interconnection interface of claim 2

wherein the first number of input address signal lines is k, the second number of independent, coded address signal lines is n, where $n > k$; and

wherein the coded addresses are n-bit codewords derived from a random encoding technique, each codeword representing a randomly or pseudo-randomly chosen n-bit codeword, the number of codewords greater than or equal to the number of nanowires.

7. The nanoscale interconnection interface of claim 2

wherein the first number of input address signal lines is k, the second number of independent, coded address signal lines is n, where $n > k$; and

wherein the coded addresses are n-bit codewords derived from a random linear block encoding technique.

8. The nanoscale interconnection interface of claim 2 wherein the coded addresses are codewords derived from one of:

a random encoding technique;

a random linear block encoding technique;

a combinatoric encoding technique;

a systematic linear block code;

a non-systematic linear block code;

a systematic non-linear block code;

a non-systematic, non-linear block code;

an encoding technique that generates, from a first set of input addresses with a first average Hamming distance a second set of coded addresses with a second average Hamming distance greater than the first average Hamming distance; and

an encoding technique that generates, from a first set of input addresses with a first minimum Hamming distance a second set of coded addresses with a second minimum Hamming distance greater than the first minimum Hamming distance.

9. The nanoscale interconnection interface of claim 1 wherein selected coded address signal lines electrically control, through junctions, one or more nanowires selected from the number of nanowires, the positions of the junctions corresponding to a coded address.

10. The nanoscale interconnection interface of claim 9 wherein the selected coded address signal lines electrically control one or more nanowires through one or more diode junctions.

11. The nanoscale interconnection interface of claim 9 wherein the selected coded address signal lines electrically control one or more nanowires through one or more resistor junctions.

12. The nanoscale interconnection interface of claim 9 wherein the selected coded address signal lines electrically control one or more nanowires through one or more transistor junctions.

13. The nanoscale interconnection interface of claim 9 wherein the selected coded address signal lines electrically control one or more semiconductor nanowires by multiple gating of the one or more semiconductor nanowires.

14. The nanoscale interconnection interface of claim 1 wherein coded addresses are represented in the coded address signal lines by voltages.

15. The nanoscale interconnection interface of claim 1 wherein coded addresses are represented in the coded address signal lines by currents.

16. The nanoscale interconnection interface of claim 1 wherein coded addresses are represented in the coded address signal lines by a physical characteristic that can have at least two distinguishable states.

17. A method for interconnecting a number of input address signal lines to a number of nanowires, the method comprising:

assigning to each nanowire one or more coded addresses;

providing a nanoscale interconnection interface comprising a number of independent, coded address signal lines, the number of independent, coded address signal lines larger than the number of input address signal lines, interconnected with the number of nanowires, each nanowire addressed by the one or more coded addresses assigned to the nanowire, each coded address comprising signals carried by the coded address signal lines and derived from an input address received on the input address signal lines, the internal nanowire addresses separated by a minimum Hamming distance greater than one.

18. A nanoscale interconnection interface comprising:

a first number of input address signal lines that carry addresses separated from one another by at least a first minimum Hamming distance;

a second number of coded address signal lines; and

a third number of nanowires, each nanowire addressed by one or more coded addresses comprising signals carried by the coded address signal lines and derived from an input address received on the input address signal lines, the internal nanowire addresses separated from one another by at least a second minimum Hamming distance greater than the first average Hamming distance.

19. The nanoscale interconnection interface of claim 18 further comprising an encoder that receives an input address through the input address signal lines and outputs a coded address to the coded address signal lines.

20. The nanoscale interconnection interface of claim 19 wherein the coded addresses are derived from codewords corresponding to the input addresses, each input address and corresponding coded address both uniquely identifying one of:

a single nanowire; and

a single subset of the number of nanowires.

21. The nanoscale interconnection interface of claim 19

wherein the first number of input address signal lines is k, the second number of independent, coded address signal lines is n, where $n = k + r$; and

wherein the coded addresses are n-bit codewords derived from a systematic linear block error-control encoding technique, each codeword having k bits equivalent to an input address and r parity check bits and generated by multiplication of the input address by a generator matrix for the linear block code, the coded addresses separated by a minimum Hamming distance greater than 1.

22. The nanoscale interconnection interface of claim 19

wherein the first number of input address signal lines is k, the second number of independent, coded address signal lines is n, where $n > k$; and

wherein the coded addresses are n-bit codewords derived from a combinatoric encoding technique, each codeword representing a selection of a number of bits s having a value "1" within an n-bit codeword, the number of codewords C_s^n greater than or equal to the number of nanowires.

23. The nanoscale interconnection interface of claim 19

wherein the first number of input address signal lines is k, the second number of independent, coded address signal lines is n, where $n > k$; and

wherein the coded addresses are n-bit codewords derived from a random encoding technique, each codeword representing a randomly or pseudo-randomly chosen n-bit codeword, the number of codewords greater than or equal to the number of nanowires.

24. The nanoscale interconnection interface of claim 19

wherein the first number of input address signal lines is k, the second number of independent, coded address signal lines is n, where $n > k$; and

wherein the coded addresses are n-bit codewords derived from a random linear block encoding technique.

25. The nanoscale interconnection interface of claim 19 wherein the coded addresses are codewords derived from one of:

a random encoding technique;

a random linear block encoding technique;

a combinatoric encoding technique;

a systematic linear block code;

a non-systematic linear block code;

a systematic non-linear block code;

a non-systematic, non-linear block code;

an encoding technique that generates, from a first set of input addresses with a first average Hamming distance a second set of coded addresses with a second average Hamming distance greater than the first average Hamming distance; and

an encoding technique that generates, from a first set of input addresses with a first minimum Hamming distance a second set of coded addresses with a second minimum Hamming distance greater than the first minimum Hamming distance.

26. The nanoscale interconnection interface of claim 18 wherein selected coded address signal lines electrically control, through junctions, one or more nanowires selected from the number of nanowires, the positions of the junctions corresponding to a coded address.

27. The nanoscale interconnection interface of claim 26 wherein the selected coded address signal lines electrically control one or more nanowires through one or more diode junctions.

28. The nanoscale interconnection interface of claim 26 wherein the selected coded address signal lines electrically control one or more nanowires through one or more resistor junctions.

29. The nanoscale interconnection interface of claim 26 wherein the selected coded address signal lines electrically control one or more nanowires through one or more transistor junctions.

30. The nanoscale interconnection interface of claim 26 wherein the selected coded address signal lines electrically control one or more semiconductor nanowires by multiple gating of the one or more semiconductor nanowires.

31. The nanoscale interconnection interface of claim 18 wherein coded addresses are represented in the coded address signal lines by voltages.

32. The nanoscale interconnection interface of claim 18 wherein coded addresses are represented in the coded address signal lines by currents.

33. The nanoscale interconnection interface of claim 18 wherein coded addresses are represented in the coded address signal lines by a physical characteristic that can have at least two distinguishable states.

34. A method for interconnecting a number of input address signal lines to a number of nanowires, the method comprising:

assigning to each nanowire one or more coded addresses;

providing a nanoscale interconnection interface comprising a number of independent, coded address signal lines, the number of independent, coded address signal lines interconnected with the number of nanowires, each nanowire addressed by the one or more coded addresses assigned to the nanowire, each coded address comprising signals carried by the coded address signal lines and derived from an input address received on the input address signal lines by one of

a random encoding technique,

a random linear block encoding technique,

a combinatoric encoding technique,

a systematic linear block code,

a non-systematic linear block code,

a systematic non-linear block code,

a non-systematic, non-linear block code,

an encoding technique that generates, from a first set of input addresses with a first average Hamming distance a second set of coded addresses with a second average Hamming distance greater than the first average Hamming distance, and

an encoding technique that generates, from a first set of input addresses with a first minimum Hamming distance a second set of coded addresses with a second minimum Hamming distance greater than the first minimum Hamming distance.

35. The method of claim 34 further including deriving the coded addresses from codewords corresponding to the input addresses, each input address and corresponding coded address both uniquely identifying one of:

a single nanowire;

a single, unique subset of the number of nanowires; and

overlapping subsets of the number of nanowires.

36. A method for increasing signal separation within an addressing circuit, the method comprising:

identifying and determining a number components that need to be addressed;

providing a number of input address signal lines needed for carrying a number of input addresses that address the number of components; and

providing an interconnection interface comprising a number of independent, coded address signal lines interconnected with the input address signal lines and with the number of components, each component addressed by the one or more coded addresses, each coded address, corresponding to an input address, comprising signals carried by the coded address signal lines and derived from an input address received on the input address signal lines by one of

a random encoding technique,

a random linear block encoding technique,

a combinatoric encoding technique,

a systematic linear block code,

a non-systematic linear block code,

a systematic non-linear block code,

a non-systematic, non-linear block code,

an encoding technique that generates, from a first set of input addresses with a first average Hamming distance a second set of coded addresses with a second average Hamming distance greater than the first average Hamming distance, and

an encoding technique that generates, from a first set of input addresses with a first minimum Hamming distance a second set of coded addresses with a second minimum Hamming distance greater than the first minimum Hamming distance.

37. The method of claim 36 further including deriving the coded addresses from codewords corresponding to the input addresses, each input address and corresponding coded address both uniquely identifying one of:

a single component; and

a single subset of components.